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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,268	GULBRANSEN ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9 and 11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 08/15/2007 have been fully considered but they are not persuasive.

Examiner's response:

2. Applicant argues with regards to claim 1 that Ying et al. do not disclose or suggest the use or application of any other mechanism to implement variable conversion gain (i.e., other than a variable capacitive load connected in parallel with the photodiode of a pixel) and therefore impermissible hindsight is used. The Examiner respectfully disagrees.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In this case, Ying et al. discloses in figure 2b one implementation of a variable conversion gain 202 that comprises transistor C1 and M7 (Paragraphs 21-23). Ying et al. further discloses in figure 4 another possible configuration having two capacitors (C3 and C5) and two transistors (M9 and M11). Finally Ying discusses that it is possible to have more than two legs in the variable capacitive load (Paragraph 26). Therefore Ying suggests multiple embodiments of variable capacitive loads and transistors in order to have the conversion gain of the pixel to be changed in response to several different thresholds of light intensity. Furthermore, the claim very

broadly recites "comprising a plurality of capacitances, switches and transistors that are programmably coupled".

Ying discloses these features as "a plurality of capacitances (figure 4, C3 and C5), switches (Paragraph 26 states that it is possible to have more than two legs for the variable capacitive load 202, therefore each leg will have a transistor acting as a switch and a capacitor acting as a load, so e.g. two additional legs will each have a transistor and a capacitor in series and is therefore the transistors are being read as switches) and transistors (M9 and M11) that are programmably (figure 5 shows an intensity detector circuit 205 that generates different conversion gain control signals 203 depending upon the light intensity threshold, Paragraph 22) coupled together". The claims so not recite any specific way of connecting these elements shown in figures 2 and 3 of applicant's specification. Therefore in the present form

As for the limitations of "first amplifier circuit is comprised of a Charge Transimpedance Amplifier (CTIA) input circuit, and where said second amplifier circuit is comprised of a Source Follower per Detector (SFD) input circuit", it is noted that none of the circuitry shown in figures 2 and 3 of applicant's specification is claimed except "comprising a plurality of capacitances, switches and transistors that are programmably coupled" which is very broad and Ying teaches these features. AAPA teaches a Charge Transimpedance Amplifier (CTIA) input circuit, and where said second amplifier circuit is comprised of a Source Follower per Detector (SFD) input circuit. Therefore as broadly as claimed Ying in view of AAPA discloses the claimed limitations.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 4, 5, 8, 9, 11, 12, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ying et al. (US PG-PUB # 2004/0079977) in view of Applicant's admitted prior art.

[Claim 1]

Ying et al. teaches a readout circuit unit cell (figure 4) for use with a radiation detector, comprising

a plurality of capacitances (figure 4, C3 and C5), switches (Paragraph 26 states that it is possible to have more than two legs for the variable capacitive load 202, therefore each leg will have a transistor acting as a switch and a capacitor acting as a load, so e.g. two additional legs will each have a transistor and a capacitor in series and is therefore the transistors are being read as switches) and transistors (M9 and M11) that are programmably (figure 5 shows an intensity detector circuit 205 that generates different conversion gain control signals 203 depending upon the light intensity threshold, Paragraph 22) coupled together to form one of a first amplifier circuit having a first gain state (When the circuit has three legs, the capacitance in the third leg will be added to have pixel conversion gain corresponding to C3+C5+capacitance of third leg) or a second amplifier circuit having a second gain state that differs from the first gain state (e.g. conversion gain for the pixel having a capacitance C3+C5).

Ying teaches a readout circuit that operates as a high gain amplifier and a low gain amplifier circuit but fails to teach where said first amplifier circuit is comprised of a Charge Transimpedance Amplifier (CTIA) input circuit, and where said second amplifier circuit is

comprised of a Source Follower per Detector (SFD) input circuit. However Applicant's admitted prior art teaches wherein readout circuit amplifier types include a high gain amplifier type known as the charge transimpedance amplifier (CTIA), sometimes referred to as a reset integrator, while a lower gain amplifier type is known as a source follower per detector (SFD, Page 1, Paragraphs 2 and 3). Therefore taking the combined teachings of Ying and Applicant's admitted prior art, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a first amplifier circuit is comprised of a Charge Transimpedance Amplifier (CTIA) input circuit, and where said second amplifier circuit is comprised of a Source Follower per Detector (SFD) input circuit in order to have a constant bias current while the first amplifier is used as a CTIA and a low noise preamplifier when used as a source follower detector.

[Claim 3]

Ying teaches where the first gain state is wider than the second gain state (figure 3, Paragraph 24. As the capacitances are added the gain reduces, so the first gain state is wider than the second gain state). Applicant's admitted prior art teaches wherein readout circuit amplifier types include a high gain amplifier type known as the charge transimpedance amplifier (CTIA), sometimes referred to as a reset integrator, while a lower gain amplifier type is known as a source follower per detector (SFD, Page 1, Paragraphs 2 and 3).

[Claim 4]

Ying teaches where the first gain state overlaps the second gain state (In figure 3, if line 309 is extended, it will overlap 307).

[Claim 5]

Ying teaches where said plurality of capacitances, switches and transistors are programmably coupled together to form said first amplifier circuit below an illumination level threshold, and are programmably coupled together to form said second amplifier circuit above said illumination level threshold (Paragraphs 22, 24-26).

[Claim 8]

Ying discloses a reset transistor (109) that acts as a reset for the photodiode 105 when the circuit operates in lower or higher gain mode. It is noted that since the reset transistor 109 will inherently have a resistance and due to the voltage supply Vdd, it also acts as a current source.

[Claims 11 and 16]

These are method claims corresponding to apparatus claims 3 and 8 respectively. Therefore these claims have been analyzed and rejected based upon apparatus claims 3 and 8.

[Claims 9, 12, 13]

These are method claims corresponding to apparatus claims 1, 4 and 5 respectively. Therefore these claims have been analyzed and rejected based upon apparatus claims 1, 4 and 5.

5. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ying et al. (US PG-PUB # 2004/0079977), Applicant's admitted prior art and further in view of Janesick (US Patent # 6,909,126).

[Claim 7]

Ying in view of Applicant's admitted prior art fails to teach where said SFD input circuit operates in one of at least two integration modes: a snapshot integrate-then-read (ITR) mode and a progressive scan integrate-while-read (IWR) mode. However Janesick teaches control circuitry 114 that implements progressive scan (IWR) and snap mode (col. 4 lines 50-64, figure 1).

Therefore taking the combined teachings of Ying, Applicant's admitted prior art and Janesick, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a snapshot integrate-then-read (ITR) mode and a progressive scan integrate-while-read (IWR) mode in order to have an image undisturbed by noise arising during a sequential readout process.

[Claim 15]

This is a method claim corresponding to apparatus claim 7. Therefore it has been analyzed and rejected based upon apparatus claim 7.

6. Claims 6, 14, 17, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ying et al. (US PG-PUB # 2004/0079977), Applicant's admitted prior art and further in view of Zhao et al. (US Patent # 6,727,946).

[Claim 6]

Ying in view of Applicant's admitted prior art fails to teach a sample/hold circuit for coupling the unit cell to an output bus, where said sample/hold circuit comprises said SFD input circuit. However Zhao et al. teaches sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a second source-follower SF2 (col. 1 lines 39-47, figure 1). Therefore taking the combined teachings of Ying, Applicant's admitted prior art and Zhao, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a sample/hold circuit for coupling the unit cell to an output bus, where said sample/hold circuit comprises said SFD input circuit in order to suppress 1/f noise and fixed pattern noise.

[Claim 14]

This is a method claim corresponding to apparatus claim 6. Therefore it has been analyzed and rejected based upon apparatus claim 6.

[Claims 17 and 18]

Ying et al. teaches a readout circuit unit cell (figure 4) for use with a radiation detector, comprising a plurality of capacitances (figure 4, C3 and C5), switches and transistors (M9 and M11 and also Paragraphs 25 and 26 state that that it is possible to have more legs in the variable capacitive load 202 for different light thresholds) that are programmably (figure 5 shows an intensity detector circuit 205 that generates different conversion gain control signals 203 depending upon the light intensity threshold, Paragraph 22) coupled together to form one of a first amplifier circuit having a first gain state (When the circuit has three legs, the capacitance in the third leg will be added to have pixel conversion gain corresponding to C3+C5+capacitance of third leg) or a second amplifier circuit having a second gain state that differs from the first gain state (e.g. conversion gain for the pixel having a capacitance C3+C5). Ying teaches where said plurality of capacitances, switches and transistors are programmably coupled together to form said first amplifier circuit below an illumination level threshold, and are programmably coupled together to form said second amplifier circuit above said illumination level threshold (Paragraphs 22, 24-26).

Ying teaches a readout circuit that operates as a high gain amplifier and a low gain amplifier circuit but fails to teach where said first amplifier circuit is comprised of a Charge Transimpedance Amplifier (CTIA) input circuit, and where said second amplifier circuit is comprised of a Source Follower per Detector (SFD) input circuit and an IR radiation circuit. However Applicant's admitted prior art teaches wherein readout circuit amplifier types include a

high gain amplifier type known as the charge transimpedance amplifier (CTIA), sometimes referred to as a reset integrator, while a lower gain amplifier type is known as a source follower per detector (SFD) and an IR radiation circuit (Page 1, Paragraphs 2 and 3). Therefore taking the combined teachings of Ying and Applicant's admitted prior art, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a first amplifier circuit is comprised of a Charge Transimpedance Amplifier (CTIA) input circuit, and where said second amplifier circuit is comprised of a Source Follower per Detector (SFD) input circuit in order to have a constant bias current while the first amplifier is used as a CTIA and a low noise preamplifier when used as a source follower detector

Ying in view of Applicant's admitted prior art fails to teach a sample/hold circuit for coupling the unit cell to an output bus, where said sample/hold circuit comprises said SFD input circuit. However Zhao et al. teaches sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a second source-follower SF2 (col. 1 lines 39-47, figure 1). Therefore taking the combined teachings of Ying, Applicant's admitted prior art and Zhao, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a sample/hold circuit for coupling the unit cell to an output bus, where said sample/hold circuit comprises said SFD input circuit in order to suppress 1/f noise and fixed pattern noise.

[Claim 20]

Ying discloses a reset transistor (109) that acts as a reset for the photodiode 105 when the circuit operates in lower or higher gain mode. It is noted that since the reset transistor 109 will inherently have a resistance and due to the voltage supply Vdd, it also acts as a current source.

7. Claim19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ying et al. (US PG-PUB # 2004/0079977), Applicant's admitted prior art, Zhao et al. (US Patent # 6,727,946) and further in view of Janesick (US Patent # 6,909,126).

[Claim 19]

Ying, Applicant's admitted prior art in view of Zhao fails to teach where said SFD input circuit operates in one of at least two integration modes: a snapshot integrate-then-read (ITR) mode and a progressive scan integrate-while-read (IWR) mode. However Janesick teaches control circuitry 114 that implements progressive scan (IWR) and snap mode (col. 4 lines 50-64, figure 1). Therefore taking the combined teachings of Ying, Applicant's admitted prior art, Zhao and Janesick, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a snapshot integrate-then-read (ITR) mode and a progressive scan integrate-while-read (IWR) mode in order to have an image undisturbed by noise arising during a sequential readout process.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571)-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YKA
October 27, 2007

LIN YE
SUPERVISORY PATENT EXAMINER